AMENDMENTS TO THE CLAIMS

Please cancel claim 19 without prejudice. Kindly amend claims 1, 8-10, 20, 25-28, and 33 as shown in the following listing of claims. The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Currently Amended) An apparatus for performing cryptographic operations, comprising:

fetch logic, disposed within a microprocessor, configured to receive a ~~cryptographic instruction~~single atomic cryptographic instruction as part of an instruction flow executing on said microprocessor, wherein said cryptographic instructionsingle atomic cryptographic instruction prescribes one of the cryptographic operations, and wherein said ~~cryptographic instruction~~single atomic cryptographic instruction prescribes one of a plurality of cryptographic key sizes;

translation logic, coupled to said fetch logic, configured to translate said single atomic cryptographic instruction into a sequence of micro instructions that directs said microprocessor to perform said one of the cryptographic operations; and

execution logic, disposed within said microprocessor and operatively coupled to said ~~cryptographic instruction~~single atomic cryptographic instruction, configured to execute said one of the cryptographic operations, said execution logic comprising:

a cryptography unit, configured execute a plurality of cryptographic rounds on each of a plurality of input text blocks to generate a corresponding each of a plurality of output text blocks, wherein said one of a plurality of cryptographic key sizes is prescribed by a control word that is provided to a key size controller within said cryptography unit, and wherein said key size~~a key size~~ controller, configured to employ employs said one of a plurality of cryptographic key sizes during execution of said one of the cryptographic operations.

2. (Original) The apparatus as recited in claim 1, wherein said one of the cryptographic operations further comprises:

an encryption operation, said encryption operation comprising encryption of a plurality of plaintext blocks to generate a corresponding plurality of ciphertext blocks.

3. (Original) The apparatus as recited in claim 1, wherein said one of the cryptographic operations further comprises:

a decryption operation, said decryption operation comprising decryption of a plurality of ciphertext blocks to generate a corresponding plurality of plaintext blocks.

4. (Original) The apparatus as recited in claim 1, wherein said one of a plurality of cryptographic key sizes comprises 128 bits.

5. (Original) The apparatus as recited in claim 1, wherein said one of a plurality of cryptographic key sizes comprises 192 bits.

6. (Original) The apparatus as recited in claim 1, wherein said one of a plurality of cryptographic key sizes comprises 256 bits.

7. (Original) The apparatus as recited in claim 1, wherein said one of the cryptographic operations is executed according to the Advanced Encryption Standard (AES) algorithm.

8. (Currently Amended) The apparatus as recited in claim 1, wherein said key size controller is configured to interpret a key size field within a control word which is referenced by said ~~cryptographic instructions~~single atomic cryptographic instruction.

9. (Currently Amended) The apparatus as recited in claim 1, wherein said cryptographic instructionsingle atomic cryptographic instruction is prescribed according to the instruction format for execution on an x86-compatible microprocessor.

10. (Currently Amended) The apparatus as recited in claim 1, wherein said ~~cryptographic instructions~~single atomic cryptographic instruction implicitly references a plurality of registers within said computing devicemicroprocessor.

11. (Original) The apparatus as recited in claim 10 wherein said plurality of registers comprises:

a first register, wherein contents of said first register comprise a first pointer to a first memory address, said first memory address specifying a first location in memory for access of a plurality of input text blocks upon which said one of the cryptographic operations is to be accomplished.

12. (Original) The apparatus as recited in claim 10, wherein said plurality of registers comprises:

a second register, wherein contents of said second register comprise a second pointer to a second memory address, said second memory address specifying a second location in said memory for storage of a corresponding plurality of output text blocks, said corresponding plurality of output text blocks being generated as a result of accomplishing said one of the cryptographic operations upon a plurality of input text blocks.

13. (Previously Presented) The apparatus as recited in claim 10, wherein said plurality of registers comprises:

a third register, wherein contents of said third register indicate a number of blocks within a plurality of input text blocks.

14. (Original) The apparatus as recited in claim 10, wherein said plurality of registers comprises:

a fourth register, wherein contents of said fourth register comprise a third pointer to a third memory address, said third memory address specifying a third location in memory for access of cryptographic key data for use in accomplishing said one of the cryptographic operations.

15. (Original) The apparatus as recited in claim 14, wherein said cryptographic key data comprises a cryptographic key comprising a number of bits according to said one of a plurality of cryptographic key sizes.

16. (Original) The apparatus as recited in claim 14, wherein said cryptographic key data comprises a user-generated cryptographic key schedule.

17. (Original) The apparatus as recited in claim 10, wherein said plurality of registers comprises:

a fifth register, wherein contents of said fifth register comprise a fourth pointer to a fourth memory address, said fourth memory address specifying a fourth location in memory, said fourth location comprising said initialization vector location, contents of said initialization vector location comprising an initialization vector or initialization vector equivalent for use in accomplishing said one of the cryptographic operations.

18. (Original) The apparatus as recited in claim 10, wherein said plurality of registers comprises:

a sixth register, wherein contents of said sixth register comprise a fifth pointer to a fifth memory address, said fifth memory address specifying a fifth location in memory for access of a control word for use in accomplishing said one of the cryptographic operations, wherein said control word prescribes cryptographic parameters for said one of the cryptographic operations, and wherein said control word comprises:

a key size field, configured to specify said one of a plurality of cryptographic key sizes to be employed during execution of said one of the cryptographic operations.

19. (Cancelled)

20. (Currently Amended) An apparatus for performing cryptographic operations, comprising:

a cryptography unit ~~within~~ disposed within execution logic in a microprocessor, configured to execute one of the cryptographic operations responsive to receipt of a cryptographic instructionsingle atomic cryptographic instruction within an instruction flow that prescribes said one of the cryptographic operations, wherein said ~~cryptographic instruction~~single atomic cryptographic instruction is fetched from memory by fetch logic in said microprocessor, and wherein said ~~cryptographic~~ instructionsingle atomic cryptographic instruction also prescribes a key size to be employed when executing said one of the cryptographic operations, and wherein translation logic in said microprocessor translates said single atomic cryptographic instruction into a sequence of micro instructions that directs said microprocessor to perform said one of the cryptographic operations; and

key size control logic, operatively coupled within said cryptography unit, configured to direct said device to employ said key size when performing said one of the cryptographic operations.

21. (Original) The apparatus as recited in claim 20, wherein said key size comprises 128-bits.

22. (Original) The apparatus as recited in claim 20, wherein said key size comprises 192-bits.

23. (Original) The apparatus as recited in claim 20, wherein said key size comprises 256-bits.

24. (Original) The apparatus as recited in claim 20, wherein said one of the cryptographic operations is executed according to the Advanced Encryption Standard (AES) algorithm.

25. (Currently Amended) The apparatus as recited in claim 20, wherein said key size control logic is configured to interpret a key size field within a control word which is referenced by said ~~cryptographic instruction~~single atomic cryptographic instruction.

26. (Currently Amended) The apparatus as recited in claim 20, wherein said ~~cryptographic instruction~~single atomic cryptographic instruction is prescribed according to the instruction format for execution on an x86-compatible microprocessor.

27. (Currently Amended) A method for performing cryptographic operations, the method comprising:

within a microprocessor, fetching a cryptographic instructionsingle atomic cryptographic instruction from memory that prescribes a cryptographic key size for employment during execution of one of a plurality of cryptographic operations, and translating the single atomic cryptographic instruction into a sequence of micro instructions that direct the microprocessor to perform the one of the plurality of cryptographic operations; and

within a cryptography unit disposed within execution logic in the microprocessor, executing the cryptographic instruction and employing the cryptographic key size when performing the one of the cryptographic operations.

28. (Currently Amended) The method as recited in claim 27, wherein said fetching comprises:

via a field within a control word that is referenced by the cryptographic instructionsingle atomic cryptographic instruction, specifying the cryptographic key size.

29. (Original) The method as recited in claim 28, wherein said specifying comprises:

prescribing 128 bits as the cryptographic key size.

30. (Original) The method as recited in claim 28, wherein said specifying comprises:

prescribing 192 bits as the cryptographic key size.

31. (Original) The method as recited in claim 28, wherein said specifying comprises:

prescribing 256 bits as the cryptographic key size.

32. (Original) The method as recited in claim 27, wherein said employing comprises:

executing the one of the cryptographic operations according to the Advanced Encryption Standard (AES) algorithm.

33. (Currently Amended) The method as recited in claim 27, wherein said fetching comprises:

prescribing the ~~cryptographic instructions~~single atomic cryptographic instruction according to the instruction format for execution on an x86-compatible microprocessor.